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**1. The importance of distributed grounding in combination with porous Si trenches for the reduction of I<sub>p</sub>/sup -I Si substrate**

Han-Su Kim; Kyuchul Chong; Ya-Hong Xie; Jenkins, K.A.;

Electron Device Letters, IEEE

Volume 24, Issue 10, Oct. 2003 Page(s):640 - 642

[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(411 KB) IEEE JNL**2. Effective crosstalk isolation through p<sup>+</sup> Si substrates with semi-Insulating porous Si**

Han-Su Kim; Jenkins, K.A.; Ya-Hong Xie;

Electron Device Letters, IEEE

Volume 23, Issue 3, March 2002 Page(s):160 - 162

[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(201 KB) IEEE JNL**3. A porous Si based novel isolation technology for mixed-signal integrated circuits**

Han-Su Kim; Kyuchul Chong; Ya-Hong Xie; Devincitis, M.; Itoh, T.; Becker, A.J.; Jenkins, K.A.;

VLSI Technology, 2002. Digest of Technical Papers. 2002 Symposium on

11-13 June 2002 Page(s):160 - 161

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